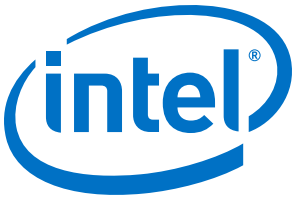

# Intel® Programmable Acceleration Card (PAC) with Intel® Arria® 10 GX FPGA Datasheet

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# Contents

# 1. Introduction

**Figure 1. Intel® PAC with Intel® Arria® 10 GX FPGA**


This datasheet for the Intel® Programmable Acceleration Card (PAC) with Intel Arria® 10 GX FPGA shows electrical, mechanical, compliance, and other key specifications. This datasheet assists data center operators and system integrators to properly deploy this PAC into their servers. It also documents the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The PAC is supported by the Acceleration Stack for Intel Xeon® CPU with FPGAs. The Acceleration Stack provides a common developer interface to both application and acceleration function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA Interface Manager (FIM).

Along with acceleration libraries and development tools, the Acceleration Stack saves development time and enables code re-use across multiple Intel FPGA form-factor products, allowing the developer to focus on the unique value-additon of their solution. Developers can use the Accelerator Functional Unit (AFU) Information Brief to get started.

The production version of the Intel Programmable Acceleration Card with Intel Arria® 10 GX FPGA will be qualified by Intel to support large scale deployments requiring FPGA acceleration. This platform is targeted for market-specific acceleration in applications such as:

- Big Data Analytics
- Artificial Intelligence
- Video Transcoding
- Cyber Security

- Genomics
- High-Performance Computing
- Finance

### Related Information

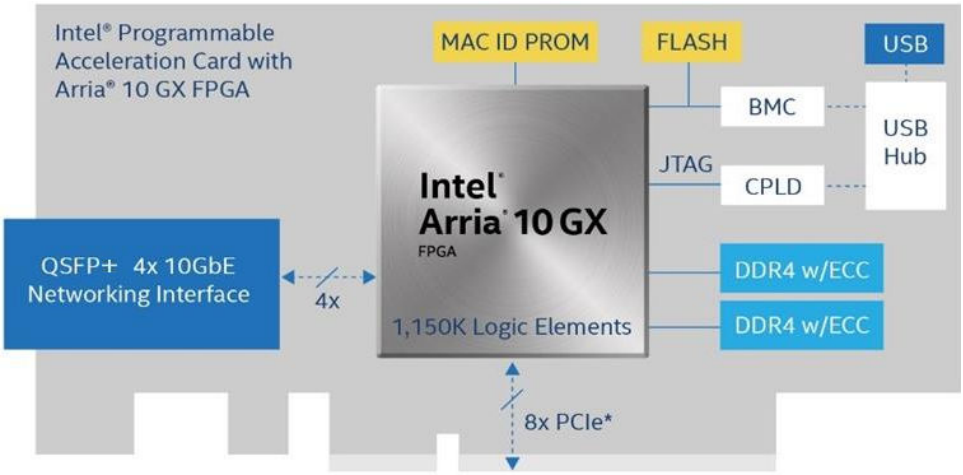
Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

# 2. Overview

This chapter provides an overview of the programmable acceleration card and describes the board architecture and its components.

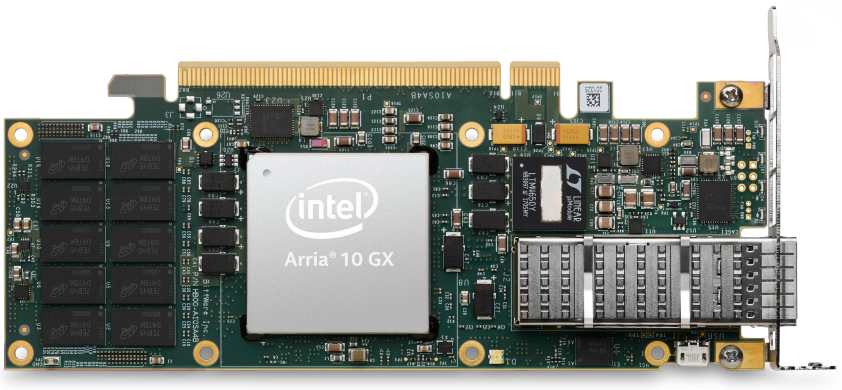
## 2.1. Block Diagram

**Figure 2. Intel PAC Block Diagram**




*Note:* The connection between the FPGA and the MAC ID PROM will be supported in a future Intel Acceleration Stack release.

**Figure 3. Intel PAC Picture**




## 2.2. Overview of Product Features

### 2.2.1. Intel Arria 10 GX FPGA

The Intel Arria 10 FPGAs feature industry-leading programmable logic built on 20 nm process technology that integrate a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Intel Arria 10 FPGAs to deliver floating point performance of up to 1.5 TFLOPS. Arria 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build versatile set of acceleration solutions.

When developing the accelerator function for the Intel PAC, select the 10AX115N2F40E2LG device.

**Related Information**

- Intel FPGA Devices
  Detailed information about features of the Intel Arria 10 GX FPGA family
- Intel Arria 10 Device Datasheet
  This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel Arria 10 devices.
- Intel Arria 10 Device Overview
  This device overview provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

### 2.2.2. On-Board Memory

- 8 GB Double Data Rate 4 (DDR-4) Memory Banks with error correction code (ECC) (2 banks) operating at 2133 Mbps. There are two banks, each of 4 GB capacity.
- The memory width is 64 data bits plus 8 ECC bits
- 1 Gb (128 MB) Flash – for use with the FIM

*Note:* Refer to the AFU Developer's Guide for access within the FIM to this memory link.

**Related Information**

AFU Developer's Guide

### 2.2.3. Interfaces and Dimensions

- PCI Express (PCIe) x8 Gen3 electrical, x16 mechanical for stability
- USB 2.0 interface for debug and programming FPGA and Flash
- 1x Quad Small Form Factor Pluggable+ (QSFP+) with 4x 10GbE or 40GbE support
- Can fit into 1 Rack Unit
- ½ Length, ½ Height with low profile bracket installed
- Standard bracket available with air duct addition available

*Note:* One rack unit is 44.5 mm (1.75 inches) high. One rack unit is commonly designated as "1U".

### 2.2.4. Software

- Acceleration Stack for Intel Xeon CPU with FPGAs
- FIM Installed

  *Note:* Certain engineering sample boards may be supplied without the FIM installed.

**Related Information**

Intel FPGA Acceleration Hub
Information about the acceleration stack

### 2.2.5. Power

- 60 W TDP and 70 W peak power
- Up to 45 W FPGA power consumption
- The PAC source power is from the PCIe* edge connector only

### 2.2.6. CPLD

The CPLD is a JTAG blaster. JTAG is used for debug and instances where the FIM image is corrupted or needs to be updated.

### 2.2.7. QSFP+

This acceleration card has a QSFP+ cage on the front panel which supports 40 GbE or four 10 GbE channels using optical transceivers. The QSFP+ interface supports many serial communication standards in addition to 40/10 GbE, including Infiniband, Fibre Channel, SONET, Common Public Radio Interface (CPRI), OBSAI, Serial RapidIO and SerialLite.

#### QSFP+ SerDes

The QSFP+ interface has four SerDes lanes connected directly to the FPGA with up to 15 Gbps operation.

*Note:* This feature will be supported in a future Intel Acceleration Stack release.

### 2.2.8. Control and Support

The following features are available on this acceleration card for configuration, control and support:

- USB
- Board Management Controller (BMC)

#### 2.2.8.1. USB

This acceleration card has a USB 2.0 port for (J1) for debug and configuration in select cases. The USB interface is used for the following:

- Read/write Intel Arria 10 FPGA configuration in Flash
- Read manufacturing data via USB
- Monitor on-board temperature and power
- Update the board's BMC firmware
- JTAG access to the Intel Arria 10 FPGA through the board's embedded USB Blaster

*Note:* The specification of the inbound hub is USB 2.0 but it auto-negotiates from a USB 3.0 host PC.

#### 2.2.8.2. Board Management Controller

A BMC is present on the PAC. The firmware is updated through the local USB. Any BMC firmware updates that are provided by Intel, OEM, ODM must be updated locally using the USB connection.

#### BMC Features

- Automatic Shut-down
- BMC default setting to shut down board at 100 °C
- Monitoring of board sensors which requires USB connectivity

You have the capability to identify whether the BMC is seeing a board failure from the two on-board LEDs. From back side of server, if you look into the bracket of the Intel PAC through venting holes, there are four steadily ON green LEDs. Behind them (further into the board), there is either a green LED or red LED that is on. The green

LED shall blink whenever BMC is operating and will be steadily on if BMC is being initialized. In the case the BMC sees a failure condition and holds off board power, typically due to overheated FPGA or too much power being drawn, a red LED (right next to green LED) will be steadily on.

# 3. System Compatibility

This section describes the platforms and Linux distribution targeted for the acceleration card validation.

*Note:* This section will be updated as Intel validates more server platforms.

### Platforms

**Table 1. Platform Validation**

| Servers/Systems | Description |
|---|---|
| Intel | Neon City (NC) |
| Dell™ | R740, R640 |

Intel platforms have Skylake-EP and Cannonlake-EP processors in combination with the Lewisburg chipset.

### Operating System Validation

**Table 2. Operating System Validation**

| Operating Systems (OS) | OS Family |
|---|---|
| RHEL™ 7.4 | RHEL |
| CentOS 7.4 | CentOS |
| KVM | Linux™ |

*Note:* The above mentioned Operating Systems are Linux Kernel 3.10

Adapters must have the following PCIe ID and power/thermal budget.

*Note:*
- VID - Vendor ID
- SVID - Sub Vendor ID
- DID - Device ID
- SDID - Sub Device ID

**Table 3. PCIe ID and Power/Thermal Budget**

| PAC | PCIe VID | PCIe DID | PCIe SVID | PCIe SDID |
|---|---|---|---|---|
| Intel PAC with Intel Arria 10 GX FPGA | 0x8086 | 0x09C4 | 0x8086 | 0x0000 |

# 4. Mechanical Information

### PAC Dimensions

- Standard height, half length PCIe card
- Low profile option available
- Card Weight with Airduct: 255 g
- Maximum component height: 14.47 mm
- PCIe x16 mechanical

**Figure 4. Acceleration Card - Standard Profile Bracket with Airduct**

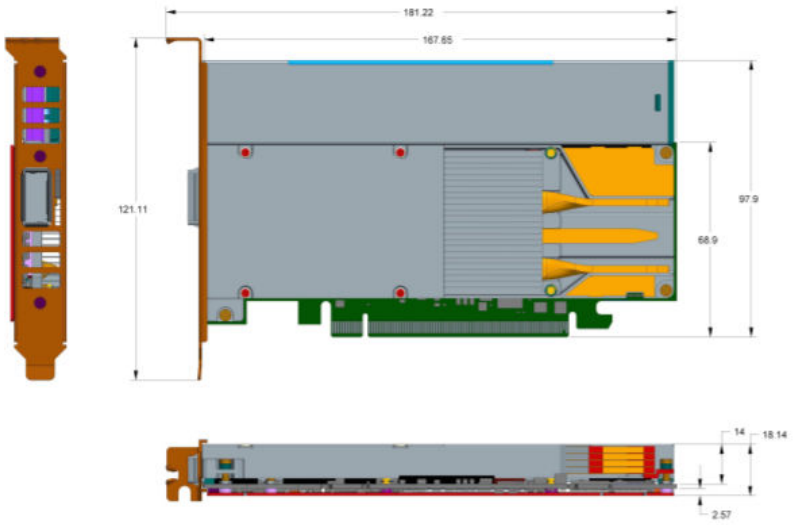


**Figure 5. Air Duct Assembly**

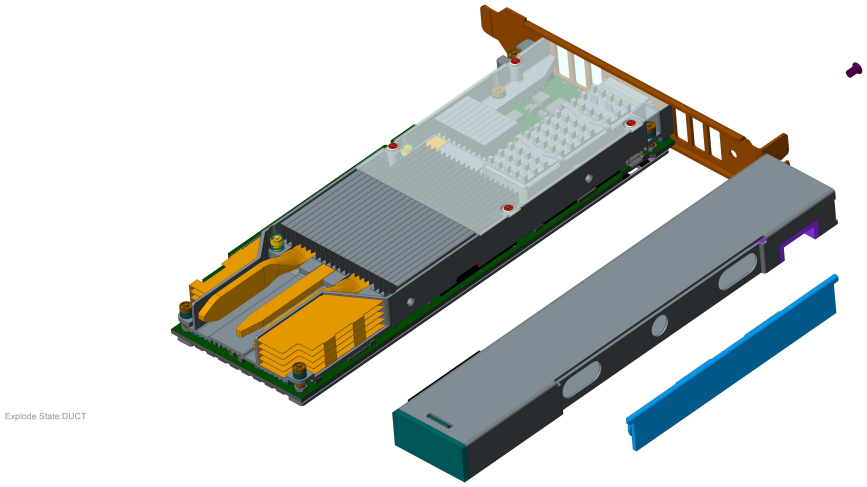



**Figure 6. Acceleration Card - Low Profile Bracket**

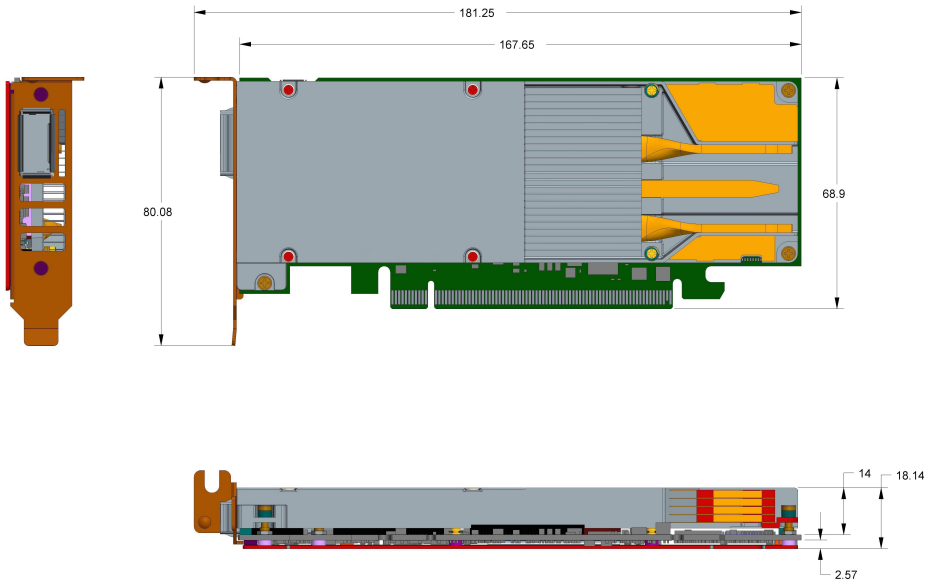
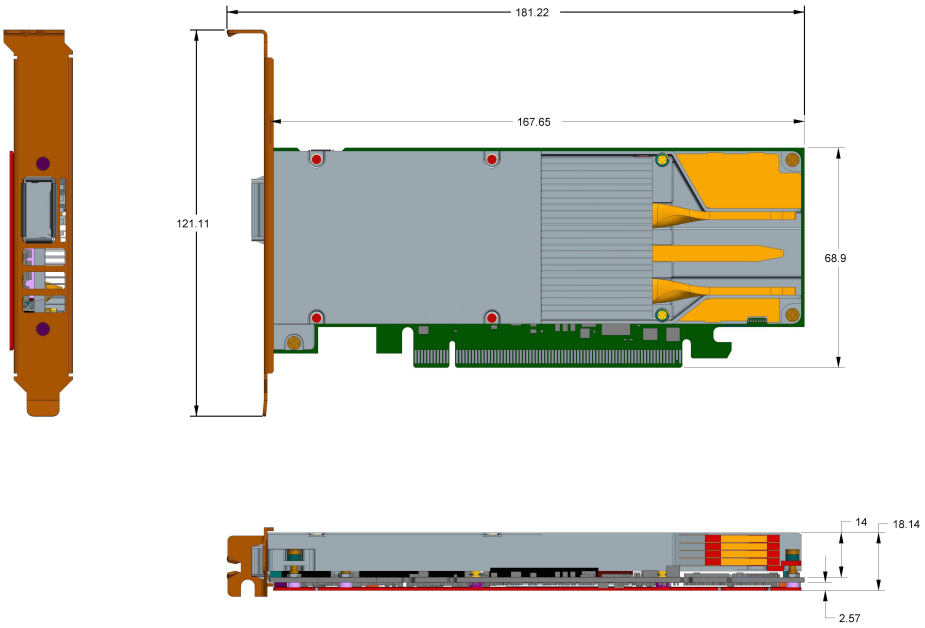


**Figure 7. Acceleration Card - Standard Profile Bracket with No Air Duct**




You can assemble or disassemble the air duct. Three screws hold the air duct in place. Two screws hold the bracket to the card and heat sink.

*Note:* Removal of air duct requires a different bracket to be used. Additional bracket options to support PAC without airduct available in Engineering Sample only.

# 5. Thermal Specifications

This acceleration card is thermally limited to dissipate no more than 45 W on the FPGA. FPGA junction temperature must not exceed 95°C. Make sure the temperature of the QSFP+ module is within the vendor specification, usually 70°C or 85°C.

- Operating Temperature: 95 °C
- Shutdown Temperature: 100 °C

*Note:* Refer to the Power Estimator Guide to avoid exceeding 95 °C.

*Note:* Intel PAC with Arria 10 GX Verification and Power Estimator User Guide describes how to verify and ensure that the AFU operates within the power supported by this card. The link to the user guide is not available and shall be provided in a future release.

*Note:* AFU Developers should use the Arria 10 PowerPlay Early Power Estimator and the Quartus Prime Power Analyzer to estimate power consumption.

**Figure 8. Airflow Pattern**


### Related Information

Intel Quartus® Prime Pro Edition Handbook Volume 1: Design and Compilation
The Intel Quartus Prime Pro Edition software provides a complete design environment for FPGA and SoC designs. The Power Analyzer is described in the Intel Quartus Prime Pro Edition Handbook.

## 5.1. Thermal Test Performance Results

### Table 4. Terms and Descriptions

| Term | Description |
|---|---|
| Linear Feet per Minute (LFM) | Air velocity is calculated by dividing the volumetric flow rate by the cross-sectional area of the flow passage. |
| $T_{LA}$ | The measured ambient temperature locally surrounding the FPGA. The ambient temperature should be measured just upstream of a passive heatsink or at fan inlet for an active heatsink. |

### Table 5. $T_{LA}$ vs. Velocity Profile with Air Duct

| $T_{LA}$ (°C) | Velocity (LFM) (85 °C QSFP spec) | Velocity (LFM) (70 °C QSFP spec) |
|---|---|---|
| 30 | 270 | 270 |
| 35 | 300 | 300 |
| 40 | 360 | 360 |
| 45 | 420 | 420 |
| 50 | 510 | 510 |
| 55 | 660 | 690 |

### Table 6. $T_{LA}$ vs. Velocity Profile without Air Duct

| $T_{LA}$ (°C) | Velocity (LFM) (85 °C QSFP spec) | Velocity (LFM) (70 °C QSFP spec) |
|---|---|---|
| 30 | 330 | 330 |
| 35 | 390 | 390 |
| 40 | 420 | 420 |
| 45 | 510 | 510 |
| 50 | 600 | 630 |
| 55 | 810 | 870 |

# 6. FPGA Interface Manager

The FPGA Interface Manager (FIM) contains the FPGA logic to support the accelerators, including the PCIe IP core, the Core Cache Interface protocol (CCI-P) fabric, the onboard DDR memory interface, and management engine. Specific features of the FIM are listed in the following documents:

- Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
- OPAE Intel FPGA Linux Device Driver Architecture Guide—Describes the architecture of the Acceleration Stack

The 1024 Mb flash memory stores the FPGA Interface Manager (FIM) which provides a common user interface for placement of accelerator functions. In addition, the FIM allows dynamic downloading of new accelerator functions and updates to the FIM.

FIM has the capability to read the FPGA temperature through the Intel Acceleration Stack.

## 6.1. Updating the FIM

The FIM image in flash memory can be updated using the following methods:

- The primary method is for the FIM to be updated over PCIe via the Acceleration Stack program `fpgaflash`. This loads the FIM image into the onboard flash memory. Upon power up, the board loads the image from flash onto the FPGA.
- Directly configure the FPGA via JTAG through the USB port. This use case should only be used if the FIM image gets corrupted or erased.

*Note:* Please refer to the Intel Acceleration Stack Quick Start Guide for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA for instructions on updating the FIM.

# A. Regulatory Information

## A.1. Japan VCCI-A Statement

この装置は、クラスA情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。 VCCI－A

## A.2. Korea EMI Statement

사용자 안내문 :A급 기기

이 기기는 업무용으로 전자파적합등록을 받은 기기이오니, 판매자 또는 사용자는 이 점을 주의 하시기 바라며, 만약 잘못 구입 하셨을 때에는 구입한 곳에서 비업무용으로 교환 하시기 바랍니다.

## A.3. United States FCC Statement

This device complies with Part 15 of the United States Federal Communications Commission (FCC) Rules. Operation is subject to the following two conditions:

1. This device may not cause hanrful interference
2. This device must accept any interefrence received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digitial device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and use in accordance with the instructions, may cause harnful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment, does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

## A.4. Canada EMC Statement

**Class A: CAN ICES-3 (A)/NMB-3(A)**

## A.5. Product Ecology

## A.6. Contact Intel Corporation

Intel Corporation

ATTN: Corporate Quality

2200 Mission College Blvd.

Santa Clara, CA 95054

USA

# B. References

### Related Information

Intel Arria 10 GX/GT Device Errata and Design Recommendations

This errata sheet provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

# C. Document Revision History for Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GX FPGA Datasheet

| Document Version | Changes |
|---|---|
| 2018.04.11 | Updated the following sections:<br>• Block Diagram on page 5<br>• On-Board Memory on page 7<br>• QSFP+ on page 8<br>• Power on page 7<br>• Board Management Controller on page 8<br>• System Compatibility on page 10<br>• Mechanical Information on page 11<br>• Thermal Specifications on page 14 |
| 2018.01.22 | Updated the following sections:<br>• Introduction on page 3<br>• Block Diagram on page 5<br>• On-Board Memory on page 7<br>• Interfaces and Dimensions on page 7<br>• Power on page 7<br>• CPLD on page 7<br>• Board Management Controller on page 8<br>• Mechanical Information on page 11<br>• Thermal Test Performance Results on page 15<br>• Regulatory Information on page 17 |
| 2017.11.03 | Engineering Sample (ES) Release |